REMARKS

Reconsideration of the present application is respectfully requested. Claims 1-11, 18-21 and 28-30 previously presented for examination remain in the application. Claims 1, 6, 10-11, 18-21 and 28 have been amended. New claims 31-38 have been added.

The Drawings stand objected to as being considered not to include every feature of the invention specified in the claims. Specifically, it is considered that the drawings do not show the claimed receiver in a clock distribution network and a duty cycle correction circuit at the receiver as recited in claim 1.

Applicants respectfully submit that the Drawings as submitted do illustrate the claimed feature. For example, **Figure 6** shows a final global clock buffer 600 including a duty cycle correction circuit 605 and/or 610 within the final global clock buffer. The Specification clearly indicates at page 4, lines 13-15, that a final global clock buffer 600 is a receiving point in the clock distribution network and at page 3, lines 17-20 that the term receiving point is used interchangeably with receiver to refer to a location in a clock distribution network at which a distributed clock signal is received and at which a local clock signal may be generated.

Further, it is considered that the drawings do not show the claimed feedback path between the input and output of the duty cycle correction circuit. Applicants respectfully submit that Figure 2 clearly illustrates the claimed feedback path between the input and output of the duty cycle correction circuit.

As described in the Specification at page 11, lines 1-4, the signal path that includes the inverter 249 and a differential sense amplifier 251 is referred to as the feedback path. As shown in Figure 2, the feedback path including the inverter 249 and the differential sense amplifier 251 is between the input 215 to the duty cycle correction circuit and the output 227 of the circuit.

Based on the foregoing, applicants respectfully submit that the Drawings meet the requirements of 37 C.F.R. § 1.83(a).

The Specification stands objected to because the Abstract is considered to use words that can be implied. More specifically, the term "is provided" is objected to. Applicants have amended the Specification as indicated above to replace the word "provided" with "located." Applicants respectfully submit that that Abstract is in the proper form.

Claims 1-5 stand rejected under 35 U.S.C. § 112, second paragraph as being considered to be indefinite for failing to particularly point out and distinctly claim the subject matter that Applicants regard as the invention. More specifically, it is stated that it is unclear from claim 1 whether the clock distribution network receives the distributed clock signal or the signal that is output from the duty cycle correction circuit.

Claim 1 sets forth

> a clock distribution network to distribute a clock signal on an integrated circuit chip; and
>
> a duty cycle correction circuit at a receiver in the clock distribution network, the duty cycle correction circuit to correct a duty cycle of a distributed clock signal received at the receiver.

Claim 1 does not address the signal received by the clock distribution network and therefore, the source of such a signal cannot be considered to be unclear. As clearly set forth in claim 1, the claim covers a duty cycle correction circuit at a receiver that corrects a duty cycle of a distributed clock signal (i.e. a clock signal from a clock distribution network) that is received by the receiver. Applicants respectfully submit that the claims meet the requirements of 35 U.S.C. § 112.

Claims 1-11, 18-21 and 28-30 stand rejected under 35 U.S.C. § 102(b) as being considered to be anticipated by U.S. Patent No. 5,008,636 to Markinson et al. ("Markinson").

Claim 1 includes the limitations

> a clock distribution network to distribute a clock signal on an integrated circuit chip; and
> a duty cycle correction circuit at a receiver in the clock distribution network, the duty cycle correction circuit to correct a duty cycle of a distributed clock signal received at the receiver.

(Claim 1)(emphasis added).

Applicants respectfully submit that Markinson does not teach or suggest the claimed features of applicants' invention including at least a clock duty cycle correction circuit at a receiver in a clock distribution network on an integrated circuit chip.

Markinson in concerned with an apparatus for low skew system clock distribution and generation of 2X frequency clocks. In accordance with Markinson, a clock generation circuit is provided on each circuit board of a

computer system to remove board-to-board system skew in clock signal distribution.

Markinson is concerned with system-level clock distribution and does not teach or suggest providing a duty cycle correction circuit at a receiving point in a clock distribution network on an integrated circuit chip.

For at least this reason, claim 1 is patentably distinguished over the Markinson reference.

Independent claims 6, 18 and 28 include a limitation similar to that argued above in reference to claim 1. Claims 2-5 and new claims 31-38, claims 7-11, claims 19-21 and claims 29-30 depend from and further limit claims 1, 6, 18 and 28. Thus claims 2-5, 6-11, 18-21 and 29-38 should also be found to be patentably distinguished over Markinson for at least the same reasons.

Based on the foregoing, applicants respectfully submit that the applicable rejections and objections have been overcome and claims 1-11, 18-21, and 29-38 are in condition for allowance. If the examiner disagrees or believes that further discussion will expedite prosecution of this case, the examiner is invited to telephone applicants' representative at the number indicated below.

If there are any charges, please charge Deposit Account No. 02-2666.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION

A clock duty cycle correction circuit. The duty cycle correction circuit is [provided] located at a receiver in a clock distribution network to correct a duty cycle of a distributed clock signal.

IN THE CLAIMS

1. (Amended) An apparatus comprising:

a clock distribution network to distribute a clock signal on an integrated circuit chip; and

a duty cycle correction circuit at a receiver in [a] the clock distribution network, the duty cycle correction circuit to correct a duty cycle of a distributed clock signal received at the receiver.

6. (Amended) A clock distribution network comprising:

clock generation circuitry at a first location to generate a global clock signal;

clock distribution circuitry to distribute the global clock signal on an integrated circuit chip from the clock generation circuitry to a receiving point at a second, different location on the integrated circuit chip; and

a duty cycle correction circuit at the receiving point to correct the duty cycle of the distributed global clock signal received via the clock distribution circuitry.

10. (Amended) The clock distribution network of claim 9 wherein a signal communicated via the feedback path in the duty cycle correction circuit is to control[s] at least one variable delay element in the duty cycle correction circuit.

11. (Amended) The clock distribution network of claim 6 wherein the duty cycle correction circuit provides a corrected output clock signal having a substantially 50% duty cycle.

18. (Amended) An integrated circuit [device] chip comprising:

a clock generation circuit to provide a first clock signal having a first duty cycle;

a clock distribution network coupled to the clock generation circuit to distribute the first clock signal across the integrated circuit [device] chip; and

a plurality of duty cycle correction circuits at receiving points in the clock distribution network, the duty cycle correction circuits to correct a duty cycle of the first clock signal at the receiving points.

19. (Amended) The integrated circuit [device] chip of claim 18 wherein at least one of the duty cycle correction circuits is coupled to frequency multiplying circuitry.

20. (Amended) The integrated circuit [device] chip of claim 19 wherein the duty cycle correction circuits are to correct the duty cycle of the first clock signal to be substantially a 50% duty cycle.

21. (Amended) The integrated circuit [device] chip of claim 18 wherein at least one of the duty cycle correction circuits is coupled to smart buffer circuitry to provide for proper operation of the at least one duty cycle correction circuit for a range of loads to be coupled to an output of the at least one duty cycle correction circuit.

28. (Amended) A method comprising:

receiving an input clock signal from a clock distribution network on an integrated circuit chip at an endpoint of the clock distribution network; and

correcting the duty cycle of the input clock signal at the endpoint to provide a corrected output clock signal.